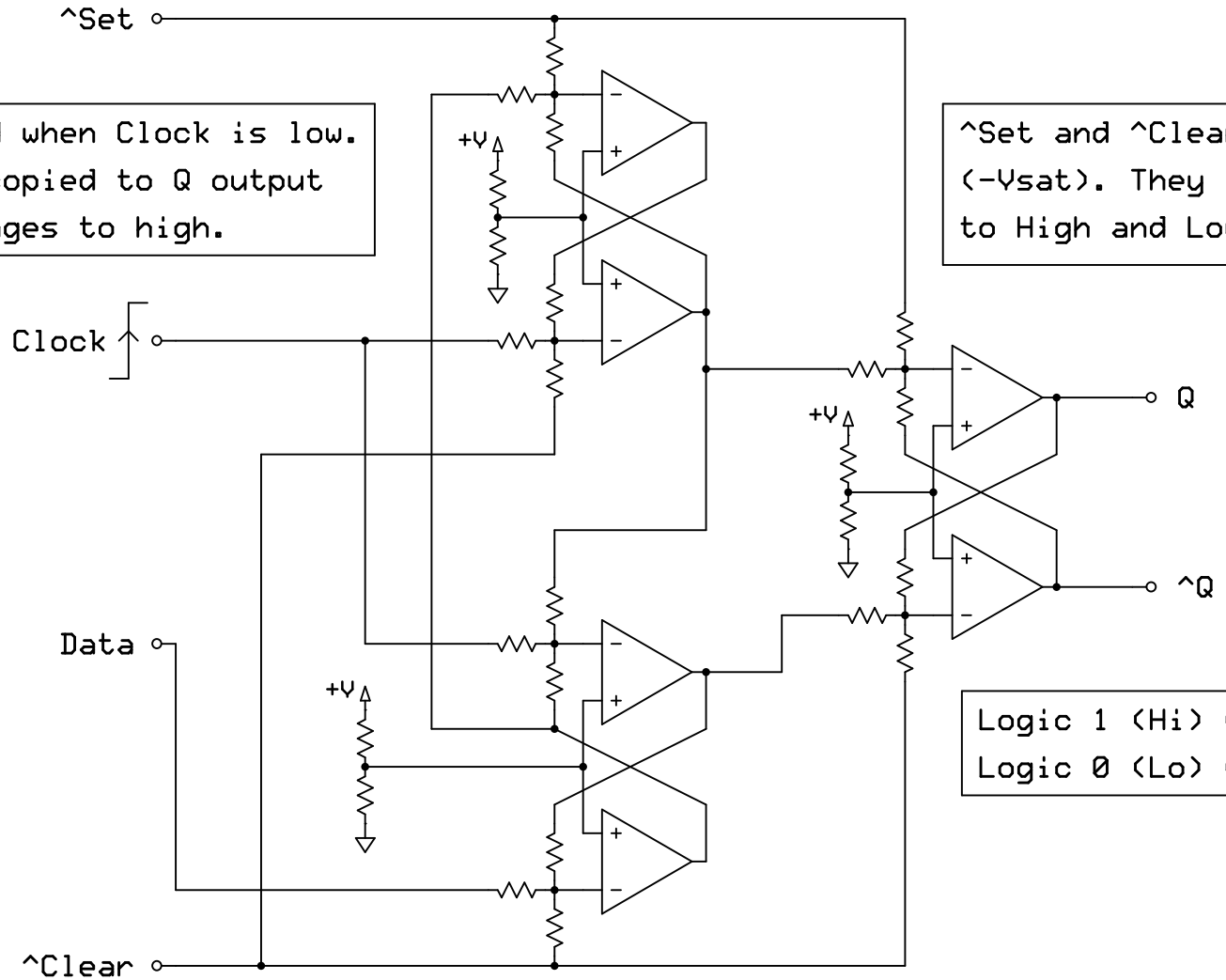
Type D (Data) Flip-Flop

Positive Edge Triggered



Data value read when Clock is low. Value is then copied to Q output when Clock changes to high.

^Set and ^Clear are active Low (-Vsat). They force Q output to High and Low, respectively.

Logic 1 (Hi) voltage is +Vsat
Logic 0 (Lo) voltage is -Vsat

All resistors have equal values >10k
Symbol +V is the positive power supply voltage
Based on TTL 74LS74A design

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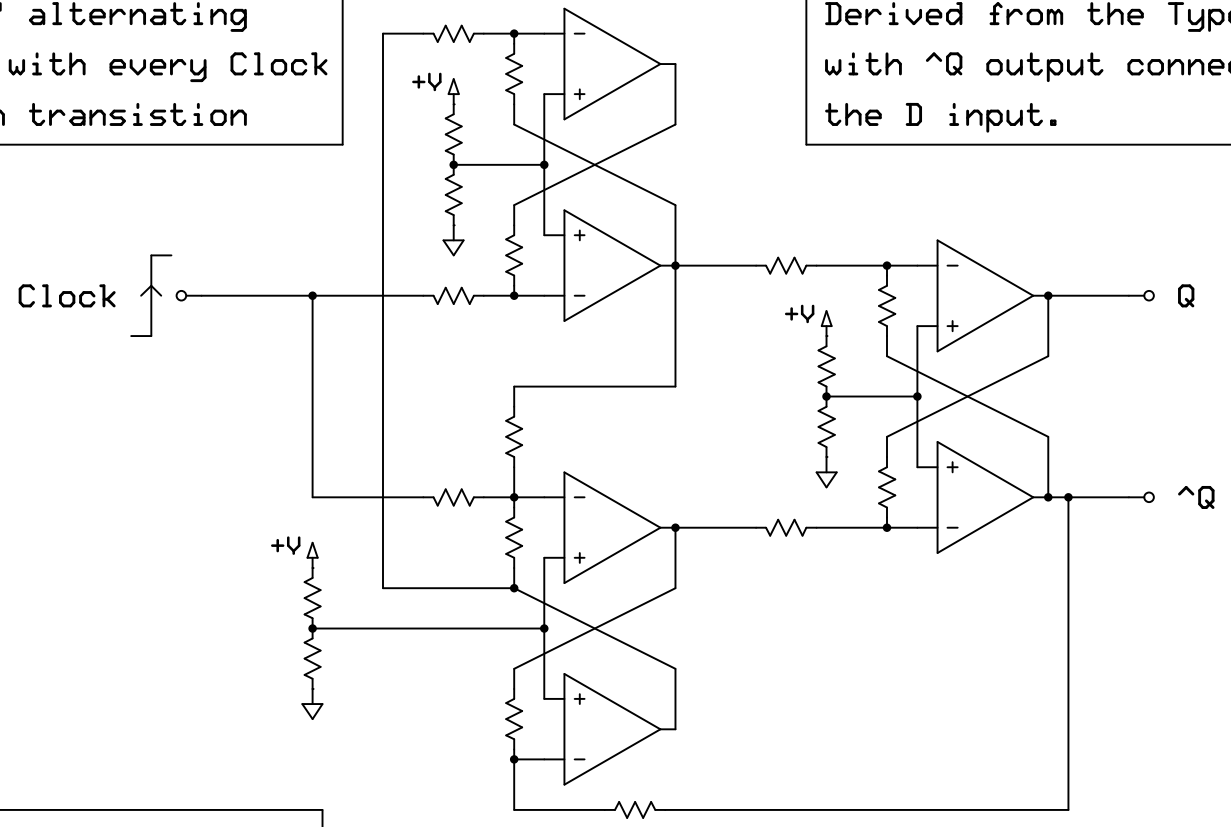
Toggled Output Flip-Flop

Positive Edge Triggered

Output "toggles," alternating between 1 and 0, with every Clock input Low -> High transistion

Derived from the Type D Flip-Flop with ^Q output connected back to the D input.



Logic 1 (Hi) voltage is +Vsat
Logic 0 (Lo) voltage is -Vsat

All resistors have equal values >10k
Symbol +V is the positive power supply voltage

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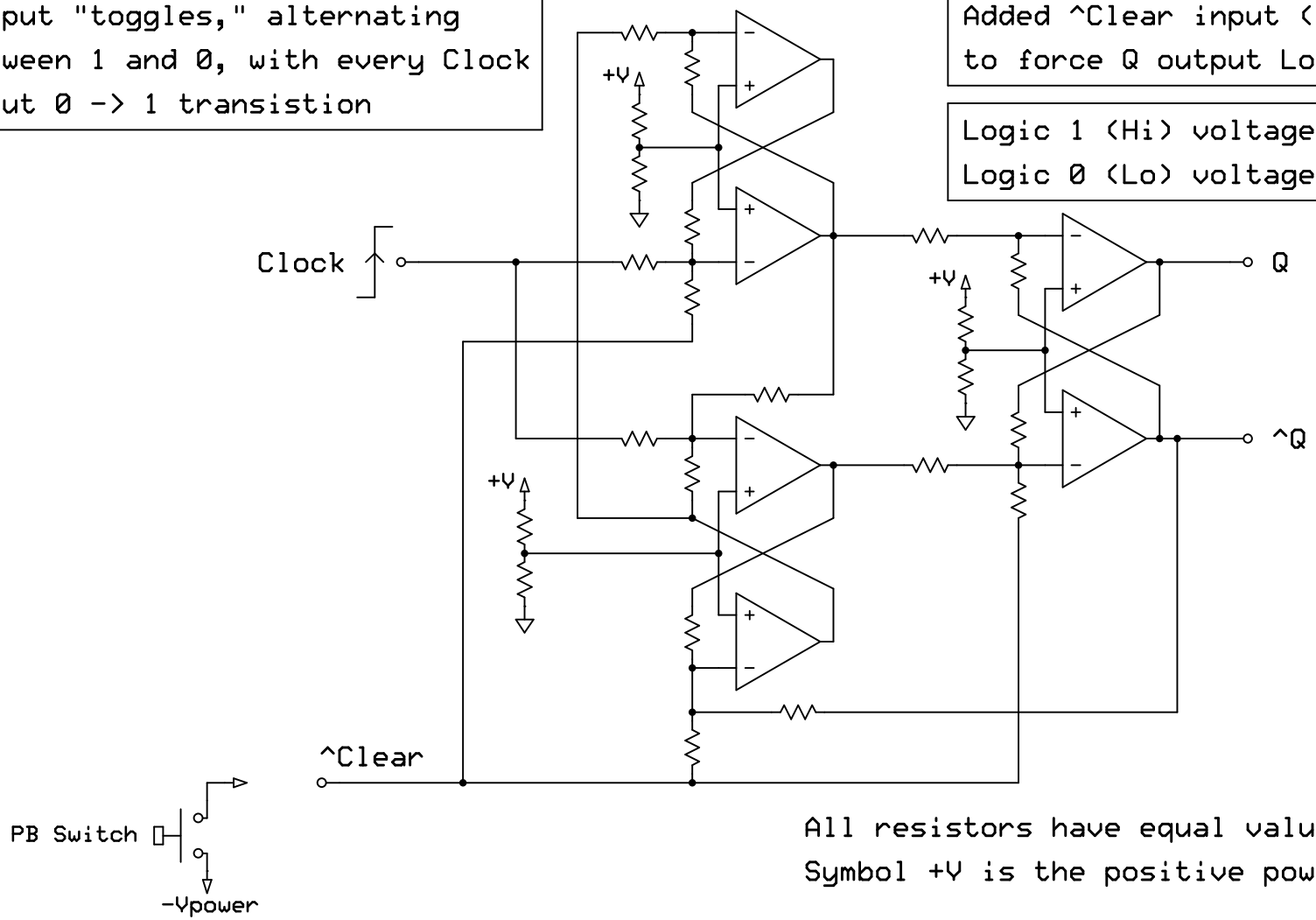
Toggled Output Flip-Flop with ^Clear

Positive Edge Triggered

Output "toggles," alternating between 1 and 0, with every Clock input 0 -> 1 transistion

Added ^Clear input (active Low) to force Q output Low (0)

Logic 1 (Hi) voltage is +Vsat
Logic 0 (Lo) voltage is -Vsat



All resistors have equal values >10k
Symbol +V is the positive power supply voltage

For manual clear, connect a push button switch between ^Clear and the negative power supply as shown.

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