Experiment 6

Transistors as amplifiers and switches

Our final topic of the term is an introduction to the transistor as a discrete circuit element. Since an integrated circuit is constructed primarily from dozens to even millions of transistors formed from a single, thin silicon crystal, it might be interesting and instructive to spend a bit of time building some simple circuits directly from these fascinating devices.

We start with an elementary description of how a particular type of transistor, the *bipolar junction transistor* (or *BJT*) works. Although nearly all modern digital ICs use a completely different type of transistor, the *metal-oxide-semiconductor field effect transistor* (*MOSFET*), most of the transistors in even modern analog ICs are still *BJT*s. With a basic understanding of the *BJT* in hand, we design simple amplifiers using this device. We spend a bit of time studying how to properly *bias* the transistor and how to calculate a transistor amplifier's gain and input and output impedances.

Following our study of amplifiers, we turn to the use of the *BJT* as a *switch*, a fundamental element of a digital logic circuit. Single transistor switches are useful as a way to interface a relatively low-power op-amp comparator output to a high-current or high-voltage device. These switches are also very useful to *translate* the output of an op-amp comparator to the proper 1 and 0 voltage levels of a standard digital logic circuit input. The final section of the text presents a few additional useful transistor applications including a discussion of a differential amplifier and a basic Class B power amplifier stage, both of which represent common building blocks of the operational amplifier.

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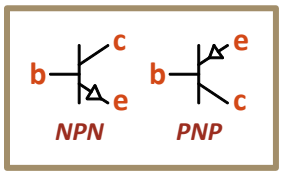
THE BIPOLAR JUNCTION TRANSISTOR

What is a transistor and how does it work?

The *bipolar junction transistor* (or *BJT*) was invented at Bell Laboratories by William Shockley in 1948, the year after he, John Bardeen, and Walter Brattain invented the first working transistor (for which they were awarded the 1956 Nobel Prize in physics). It is constructed from a sandwich of three layers of doped semiconductor material, the thin middle layer being doped oppositely from the other two. Thus there exist two types of *BJT*: *NPN* and the *PNP*, whose schematic symbols are shown at right. The three layers are called the *emitter*, *base*, and *collector*, and their identification with the three schematic device terminals is also illustrated in the figure (note that the *emitter* is associated with the *arrow* in the schematic symbols). The base is the thin middle layer, and it forms one *PN* junction with the heavily-doped emitter and another with the lightly-doped collector. When used as an amplifier, the base-emitter junction is forward-biased,



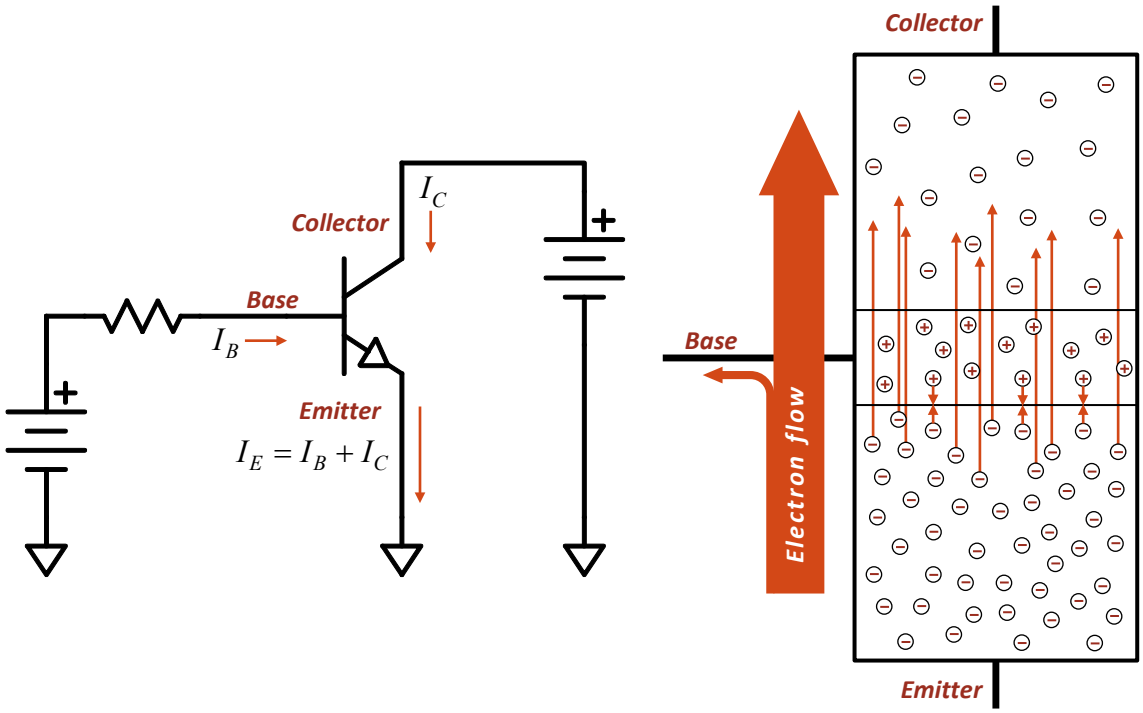


Figure 6-1: The inner workings of an *NPN* bipolar junction transistor. This transistor may be thought of as a "sandwich" of a thin *P*-type semiconductor layer (the *base*) between two *N*-type layers (the *emitter* and the *collector*). The emitter is very heavily doped with *N*-type charge carriers (conduction electrons). When the base-emitter *PN* junction is forward biased current flows from the base to the emitter. Because the base is very thin and the emitter is heavily doped, most of the emitter's charge carriers (electrons) which diffuse into the *PN* junction continue right on through it and into the collector. This results in a current flow from collector to emitter which can be much larger than the current flow from base to emitter.

whereas the collector-base junction is reverse-biased (in the case of an *NPN* transistor, the collector would be at the most positive voltage and the emitter at the most negative). The resultant charge carrier flows within the *NPN* transistor are illustrated in Figure 6-1.

Consider an *NPN* transistor's behavior as shown in Figure 6-1. When the base-emitter *PN* junction is forward-biased, a current flows into the base and out of the emitter, because this pair of terminals behaves like a typical *PN* junction semiconductor diode. The voltage drop from base to emitter is thus that of a typical semiconductor diode, or about 0.6–0.7V (nearly all transistors use silicon as their semiconductor). If the collector's potential is set more than a few 1/10ths of a volt higher than that of the base, however, an interesting effect occurs: nearly all of the majority charge carriers from the emitter which enter the base continue right on through it and into the collector!

The electrons from the *N*-type emitter that enter the base then diffuse around randomly in the *P*-type base's semiconductor material. Because the base is thin and the emitter has a large concentration of charge carriers (it is heavily doped), many electrons from the emitter approach the collector-base *PN* junction before they have a chance to recombine with the much smaller concentration of base charge carriers (holes in the case of an *NPN* transistor). The external bias voltage applied to the collector will then accelerate these emitter charge carriers across the collector-base *PN* junction. Consequently, most of the emitter charge carriers crossing the forward-biased base-emitter junction enter the collector, where they intermingle with the collector's lower concentration of similar charge carriers (Figure 6-1).

The transistor's design then ensures that most of the emitter's charge carriers which enter the forward-biased base-emitter *PN* junction wind up passing through the base and entering the collector. This charge carrier flow out of the emitter is the microscopic origin of the current that flows through the emitter's terminal on the transistor (I_E in Figure 6-1). The small fraction of these emitter charge carriers that recombine in the base then determines the fraction of the emitter current which flows through the base terminal (I_B), whereas the much larger fraction passing through the base and entering the collector determines the collector current (I_C). On the other hand, if the base-emitter *PN* junction is not forward-biased then the charge carrier flow from the emitter across the junction does not occur, and the collector-emitter current vanishes (the only currents through the device are now the tiny reverse leakage currents across the *PN* junctions).

The end result is that if we bias the transistor so that its base-emitter *PN* junction is forward-biased (base about 0.7V more positive than the emitter for an *NPN* transistor), then a small current flow in the base terminal corresponds to a much larger current flow in the collector terminal: the *BJT* transistor is a *current amplifier* (of course, the collector terminal must be connected to a power supply of some sort to complete an external circuit between collector and emitter as shown in Figure 6-1 — the power supply provides the energy required to move the current around this circuit).

The relationship between the base and collector currents: β (h_{fe})

It turns out that if the collector is at a potential of at least about 0.2V more than the base, then the ratio of the collector and base currents in a well-designed BJT transistor is remarkably independent of the magnitude of the base current and the collector-emitter voltage difference.

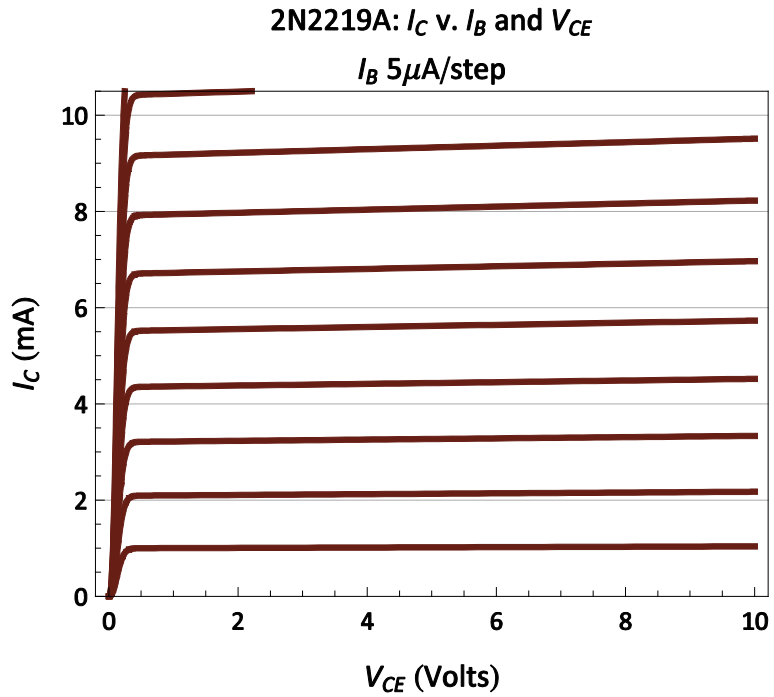


Figure 6-2: *Characteristic curves* of a typical *BJT*. The 2N2219A is a general-purpose, *NPN* transistor similar to the PN2222. Each curve shows the variation in collector current with the voltage between the collector and emitter for a fixed base current; base current was stepped through a range of values to generate the family of curves shown. The curves are nearly evenly-spaced and flat for V_{CE} > 0.8V, showing that the transistor's collector/base *current gain* (called β or h_{fe}) is nearly constant over the parameter space shown.

This behavior of a good *BJT* is strikingly illustrated by the family of collector *characteristic curves* plotted in Figure 6-2 for the *NPN* type 2N2219A transistor. Each curve in the family shows the collector current (I_C) as a function of collector-emitter voltage drop (V_{CE}) for a fixed value of base current (I_B); the base current is stepped by increments of 5 µA to generate the various curves. Note how flat the various curves are for $V_{CE} > 0.8\,\text{V}$, showing that the collector current I_C is nearly independent of V_{CE} in this regime. Next note how evenly spaced the curves are (again, for $V_{CE} > 0.8\,\text{V}$), showing how very nearly proportional the collector and base currents are. The ratio $\Delta I_C / \Delta I_B$ defines the transistor's *current gain*, commonly designated variously by the symbols β (*beta*) and h_{fe} (the more "formal," engineering symbol for this parameter). Referring back to Figure 6-1, the current gain is clearly just the ratio of the number of emitter charge carriers which continue on to the collector to the number which recombine in the base. For the 2N2219A transistor shown in Figure 6-2, β averages about 250 (it rises a bit with increasing I_B); a well-designed, general-

purpose transistor will have $\beta \gg 1$. Unfortunately, for a given transistor β is a strong function of temperature, rising by about 10% for a 10°C rise in temperature; it also can vary by as much as 30% between transistors with the same model number. This possible variance in β should be considered when designing transistor amplifiers.

The transistor as an amplifier

Consider the circuit fragment shown at right, which includes an *NPN* transistor connected between two power supply "*rails*" V_{CC} and V_{EE} (with, naturally, $V_{CC} > V_{EE}$). Assume that some method has been used to *bias* the transistor's base terminal at the voltage $V_B > V_{EE}$ so that the transistor's base-emitter junction is forward-biased and is therefore conducting current I_B as shown (we'll discuss ways of biasing the transistor in a subsequent section). What we want to determine are the relationships between the various voltages and currents, the resistor values R_C and R_E, and the transistor's β.

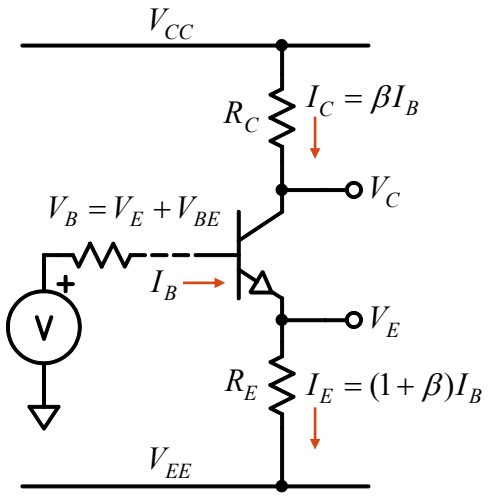


Figure 6-3: A collector-emitter circuit fragment of an *NPN* transistor used as an amplifier.

We start the analysis by relating the base and emitter voltages using the forward-bias diode drop $V_{BE} \approx 0.6\text{V}$ across the base-emitter *PN* junction. As we know from our previous study of the semiconductor diode, this voltage will be a very weak function of the base current I_B, so we will use the working assumption that it is a fixed, constant value. Consequently, if we know V_B then we also know V_E and vice versa. Given V_E, we now know the voltage drop across resistor R_E, so we also know the current through it: $I_E = (V_E - V_{EE})/R_E$.

Knowing I_E and the transistor's current gain β immediately tells us the other two transistor currents I_B and I_C, since the three currents are related through β as shown in Figure 6-3. The value of R_C then gives us the collector voltage V_C, since $I_C = (V_{CC} - V_C)/R_C$. Thus we have succeeded in relating the circuit's state variables (currents and voltages), as we set out to do. Note that there are some conditions that must be met for our solution to be realistic: all the currents must flow in the directions shown by the arrows in Figure 6-3, and it must be the case that $V_{EE} < V_E < V_B \le V_C < V_{CC}$. If one or more of these conditions is violated by our solution, then our solution fails, and the transistor circuit is operating as a *switch* rather than as an *amplifier* (we'll discuss transistor switch circuits in a later section).

Now consider how V_E and V_C are affected by a small change dV_B in the transistor's base voltage. If the solution we have found is perturbed by changing the transistor base bias voltage from V_B to $V_B + dV_B$, then the emitter voltage will change by the same amount,

since we assume that V_{BE} is constant. Thus $dV_E = dV_B$, and the *small-signal voltage gain* of the circuit in Figure 6-3 from the base to the emitter of the transistor is:

6.1 Emitter follower voltage gain: $G \equiv dV_E / dV_B = 1$

A transistor amplifier circuit used in this way is called an *emitter follower*, analogous to the op-amp voltage follower circuit, since the voltage gain of the circuit is 1.

The change dV_E in the emitter voltage will change the emitter current as well because the voltage drop across R_E has changed, so $dI_E = dV_E / R_E$; this changes the collector current to $dI_C = dI_E / (1 + 1/\beta) \approx dI_E$, because $\beta \gg 1$ (the quantity $dI_C / dI_E = 1/(1 + 1/\beta)$ is sometimes referred to as the transistor's α; clearly for a good transistor $\alpha \approx 1$). Finally, dI_C changes the voltage drop across R_C; since the power supply voltage V_{CC} is constant, the change in voltage drop across R_C will change the collector voltage by $-R_C dI_C$, and the voltage gain of the circuit from the base to the collector of the transistor is therefore:

6.2 Common-emitter voltage gain (β»1): $G \equiv dV_C / dV_B = -R_C / R_E$

This output configuration of the circuit in Figure 6-3 is called a *common-emitter amplifier*, which is an *inverting* amplifier whose gain formula resembles that of the op-amp inverting amplifier circuit. Note that just as in the case of the op-amp circuit, the ideal gain formula in (6.2) obtains as the transistor gain $\beta \to \infty$.

Next let us consider the input and output impedances of the transistor amplifier circuit fragment of Figure 6-3. The input impedance presented by the base terminal of the transistor is quite straightforward given the previous calculations. Since $Z_{in} = dV_B / dI_B$, $dV_E = dV_B$, and $(\beta + 1) dI_B = dI_E = dV_E / R_E$, we immediately see that the base input impedance is:

6.3 Base terminal input impedance: $Z_{in} = (\beta + 1) R_E \approx \beta R_E$

The output impedance at the terminal labeled V_C in Figure 6-3 is likewise easy to determine if we assume that the transistor's β is independent the collector-emitter voltage difference V_{CE} (in other words, if we assume that the characteristic curves shown in Figure 6-2 are flat and horizontal, as they very nearly are in that figure). In this case, since $Z_{out} = -dV_C / dI_{out}$ (where I_{out} is the change in the current drawn from the output terminal by some attached load), changing the load current cannot affect the current flow into the transistor's collector, because that current is determined solely by I_B. Thus any change in output current must pass through the collector resistor R_C, which therefore must be the circuit's output impedance (if the assumption regarding the characteristic curves is relaxed, then the reciprocal of the slope of the appropriate curve defines the *collector's dynamic output impedance*, and this impedance must be combined in parallel with R_C, slightly lowering the circuit's output impedance).

6.4 Common-emitter output impedance: $Z_{out} = R_C$

Finally, the emitter-follower output impedance at the terminal labeled V_E in Figure 6-3 must be determined: $Z_{out} = -dV_E / dI_{out}$. In this case, since $dV_E = dV_B$, a change in the emitter voltage will cause a corresponding change in the base voltage, which may in turn change the base bias current, I_B. Assume that the source of the bias for the transistor base has output impedance Z_S (the resistor shown in the base terminal circuit of Figure 6-3 between it and the constant bias voltage source V). The relationship between the base terminal current and voltage would then satisfy: $Z_S = -dV_B / dI_B$, so that the current out of the transistor's emitter would change as: $dI_E = (\beta + 1) dI_B = -(\beta + 1) dV_E / Z_S$. But this is not the whole story — dV_E will change the current through R_E by dV_E / R_E. Using Kirchhoff's current law, the sum of the change in current through R_E and at the output terminal dI_{out} must equal the change in current supplied by the emitter of the transistor, so:

$$-dV_E \frac{\beta + 1}{Z_S} = dI_{out} + dV_E \frac{1}{R_E} \quad \rightarrow \quad -\frac{dV_E}{dI_{out}} = \left(\frac{1}{R_E} + \frac{1}{Z_S / (\beta + 1)} \right)^{-1}$$

So the emitter follower's output impedance is the parallel combination of the circuit's *embedding impedance* seen by the transistor's base divided by $(\beta + 1) \approx \beta$ and R_E, a combination which could result in a reasonably small output impedance:

6.5 Emitter follower output impedance: $Z_{out} = \left(\frac{1}{R_E} + \frac{1}{Z_S / \beta} \right)^{-1}$

Ways to design practical transistor amplifier circuits are discussed in a later section.

BASIC TRANSISTOR AMPLIFIER DESIGN

Designing a common-emitter amplifier stage

A simple and effective way to construct a transistor gain stage is to supply the transistor's base bias using a voltage divider and to *AC couple* the input and output signals as shown in Figure 6-4. The big advantage of this circuit is that it can be designed to work successfully almost completely independently of the transistor's current gain β, so that it will work with nearly any available transistor and will be very tolerant of circuit temperature and power supply voltage variations. In this section we will go through a design procedure for this circuit so that you can successfully assign the proper values to the resistors and capacitors in the circuit.

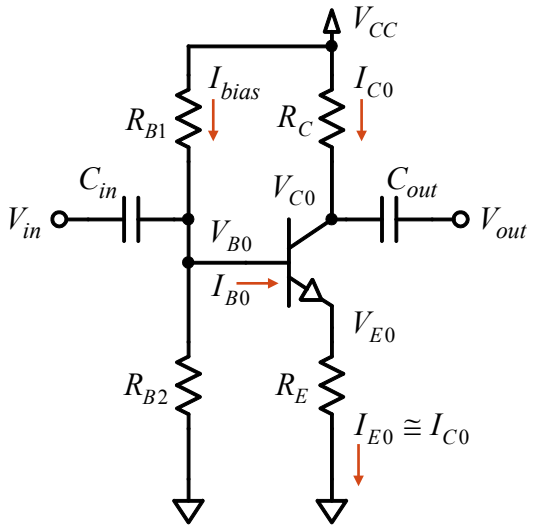


Figure 6-4: Basic *NPN* common-emitter amplifier stage. Component selection to establish the design stage gain and properly bias the transistor is discussed in the text.

In the following several sections, our calculations regarding gains and impedances assume that the input signal frequency is well within the pass-band of the input and output AC coupling filters: that is, the impedances of the capacitors C_{in} and C_{out} can be neglected at signal frequencies. Of course, the circuit behavior at 0 frequency (DC) assumes that the capacitors are open circuits.

Amplifier gain; the quiescent collector and emitter operating state

The first step is to set the required gain G of the stage. The circuit in Figure 6-4 is most effective for relatively modest gains, say $5 \le |G| \le 20$ or so; as the stage gain goes up, the circuit's input impedance will have to drop and the output impedance will rise, although these problems may be mitigated somewhat by a judicious choice of power supply voltage. If you need a large gain, you will probably have to cascade several amplifier stages to achieve this result. In any event, the target gain for each amplifier stage sets its ratio of the collector and emitter resistor values through equation (6.2): $G = -R_C / R_E$.

The next step is to establish the value of V_{CC}, the power supply voltage you will use, and the transistor's *quiescent operating state*, target values of the collector and emitter DC voltages in the absence of an input signal: V_{C0} and V_{E0} (the subscript 0 implies that these are the quiescent, DC values of these circuit parameters). These choices will be driven by the circuit gain G and the required peak-to-peak output voltage swing, V_{pk-pk}. To see how this works, the argument goes as follows:

(1) As described in the discussion leading up to the common-emitter gain equation (6.2), the ratio of the voltage drops across resistors R_C and R_E is equal to the magnitude of the amplifier stage's voltage gain $|G|$. Thus $|G| = (V_{CC} - V_C)/V_E$. This relationship will hold at all times, regardless of the signal output. When the output signal is at its positive peak, the voltages across the two resistors will be at their smallest values; when the output signal is at its negative peak, the difference $V_{CE} = V_C - V_E$ is at its minimum.

(2) To minimize distortion in the output of the amplifier, the design must keep the transistor from saturating; the voltage drop from collector to emitter V_{CE} should go no lower than about 1V (see Figure 6-2). Therefore at the negative output peak $(V_C)_{\min} - (V_E)_{\max} = 1\text{V}$. Combining this with the above relation, we get:

$$(V_E)_{\max} = (V_{CC} - 1\text{V})/(|G| + 1)$$
$$(V_C)_{\min} = (V_{CC} + |G| \times 1\text{V})/(|G| + 1)$$

(3) When the output voltage V_C is at its maximum, the collector current I_C is at its minimum. As a conservative design "rule of thumb," keep the range of collector currents reasonable by choosing the minimum collector current to be no less than about 5% of its maximum value. This restriction would, of course, apply to the emitter current as well. This design rule implies that $20 \times (V_E)_{\min} = (V_E)_{\max}$. The difference $(V_E)_{\max} - (V_E)_{\min}$ multiplied by the gain $|G|$ is the design collector voltage range, which will determine the maximum output V_{pk-pk}. Thus we have established a relationship between the gain $|G|$, power supply voltage V_{CC}, and the maximum output voltage swing V_{pk-pk}:

6.6
$$\left(1 + \frac{1}{|G|}\right) V_{pk-pk} = 0.95\,(V_{CC} - 1\text{V})$$

The middles of the ranges in V_C and V_E should then be the target quiescent collector and emitter voltages, V_{C0} and V_{E0}. These values will make sure that the full V_{pk-pk} output is available without hitting one of the voltage minimum or maximum limits:

6.7
$$V_{E0} = 0.525\,(V_{CC} - 1\text{V})/(|G| + 1)$$
$$V_{C0} = V_{CC} - |G| \times V_{E0}$$

EXAMPLE COLLECTOR AND EMITTER VOLTAGE CALCULATIONS

Assume that you want a gain –5 common-emitter amplifier operating from a single +5V power supply. What would be the maximum available output voltage swing, and what should be the quiescent collector and emitter voltages V_{C0} and V_{E0} to achieve this?

Solution:

Solving equation (6.6) for V_{pk-pk} given the specified G and V_{CC}: $V_{pk-pk} = 3.17\text{V}$. The quiescent voltages are calculated using equations (6.7): $V_{C0} = 3.25\text{V}$; $V_{E0} = 0.35\text{V}$.

Quiescent operating currents and base bias voltage

As indicated by equation (6.4), the circuit in Figure 6-4 will have an output impedance equal to R_C. The value of this resistor and the quiescent collector voltage V_{C0} establish the quiescent collector and base bias currents, I_{C0} and I_{B0}:

6.8
$$I_{C0} = \left(V_{CC} - V_{C0}\right)/R_C$$
$$I_{B0} = I_{C0}/\beta$$

The base bias voltage, V_{B0}, must be established at 1 diode-drop (0.6V–0.7V) above the emitter voltage, V_{E0}. *This is the most important step*, since V_{B0} along with the values of R_C and R_E determine the transistor's quiescent operating state: V_{C0}, V_{E0}, and I_{C0}. Using equation (6.7),

6.9
$$V_{B0} = V_{E0} + 0.7\text{V} = 0.7\text{V} + 0.525\left(V_{CC} - 1\text{V}\right)/\left(\left|G\right| + 1\right)$$

The base bias voltage divider; input impedance

To establish the critical parameter V_{B0}, the circuit in Figure 6-4 contains a voltage divider composed of resistors R_{B1} and R_{B2}. The quiescent base bias current I_{B0} will be supplied from the power supply V_{CC} through this divider, so we must carefully consider these resistor values. We want the circuit design to accommodate a fairly large variation in transistor β without significantly affecting the amplifier's performance; the only place β matters is in the second of equations (6.8). Calculate the maximum I_{B0} you might expect by picking a reasonable lower bound on β when using that equation. To keep this current from having a significant impact on the voltage divider, design it so that the current through R_{B2} is $\approx 10I_{B0}$. By doing this you ensure that variations in β and thus I_{B0} will not significantly change V_{B0}, the amplifier's most important bias parameter. This consideration and the voltage divider equation determine the values of these resistors:

6.10
$$R_{B2} = \frac{V_{B0}}{10I_{B0}}; \qquad R_{B1} = R_{B2}\left(\frac{V_{CC}}{V_{B0}} - 1\right)$$

Finally, these values determine the amplifier's input impedance, which will be the parallel combination of R_{B1}, R_{B2}, and the transistor base input impedance, which from equation (6.3)

is βR_E. Note that a large gain will tend to drive down the value of V_{B0} and thus R_{B2}, lowering the circuit's input impedance.

EXAMPLE BASE BIAS CALCULATIONS

Continuing our previous example calculations, if we choose $R_C = 750\Omega$, then that will also be the circuit's output impedance. For $G = -5$, the required $R_E = 150\Omega$. Assume that transistor $\beta \approx 150$ (minimum); the quiescent transistor currents will be, using (6.8):

$$I_{C0} = (5\text{V} - 3.25\text{V})/750\Omega = 2.3\text{mA}$$
$$I_{B0} = 2.3\text{mA}/150 = 16\mu\text{A}$$

Now we can choose the base bias resistor values using equations (6.9) and (6.10):

$$V_{B0} = 0.7\text{V} + V_{E0} = 1.05\text{V}$$
$$R_{B2} = 1.05\text{V}/(10\times 16\mu\text{A}) = 6.75\text{k}\Omega \rightarrow 6.2\text{k}\Omega$$
$$R_{B1} = 6.2\text{k}\Omega\times(5/1.05 - 1) = 23.3\text{k}\Omega \rightarrow 24\text{k}\Omega$$

Using 24kΩ and 6.2kΩ for R_{B1} and R_{B2} will introduce an error in the target V_{B0} of only 3%, which is less than the expected 5% resistor tolerances. The amplifier input impedance will be the parallel combination of the two bias resistors and βR_E, which will give only about 4kΩ.

Choosing the coupling capacitors

The DC quiescent bias voltages must be maintained at the transistor's three terminals for the amplifier in Figure 6-4 to operate properly. Therefore the input and output signals must be isolated from these DC voltages using the coupling capacitors C_{in} and C_{out}. Thus the amplifier must be *AC coupled* as originally described in Experiment 2 in the context of an op-amp amplifier. Consider the input capacitor C_{in} first. The low-frequency –3dB corner of the high-pass filter formed from C_{in} and the input impedance of the amplifier will be:

6.11
$$f_{in} = \frac{1}{2\pi Z_{in} C_{in}} = \frac{1}{2\pi C_{in}}\left(\frac{1}{R_{B1}} + \frac{1}{R_{B2}} + \frac{1}{\beta R_E}\right)$$

The output capacitor C_{out} will form another high-pass filter with the amplifier's output impedance and the input impedance of the load attached to the amplifier output:

6.12
$$f_{out} = \frac{1}{2\pi(Z_{out} + Z_{load})C_{out}} = \frac{1}{2\pi(R_C + Z_{load})C_{out}}$$

These two high-pass filters are cascaded, so the circuit's over-all response at low frequencies will be determined by the product of the two high-pass filters' responses.

High gain amplifiers: the dynamic emitter resistance r_e

It seems from equation (6.2) that the common-emitter amplifier gain could be made arbitrarily large by reducing the emitter circuit resistor value R_E to zero (Figure 6-3). Of course, this turns out to be incorrect. One of the assumptions leading to (6.2) is that the base-emitter diode forward voltage drop V_{BE} is constant (independent of the transistor currents); this is, of course, inaccurate because it is an increase in V_{BE} applied to the base-emitter *PN* junction which drives an increase in the current through it. Returning to Experiment 3, page 3-41, it explained how the *diode equation* relates the voltage and current through a *PN* junction:

6.13
$$I_E = I_0 (e^{q_e V_{BE}/k_B T} - 1)$$

We use the emitter current I_E in this equation because that quantity represents the total current through the base-emitter *PN* junction. The characteristic current $I_0 \sim 10^{-10}\,\text{mA}$; at room temperature and with $V_{BE} \sim 0.6\text{V}$, the exponential term is $\sim e^{24} > 10^{10}$, which is ridiculously larger than 1, so the -1 term in (6.13) may be very safely ignored! Thus the *dynamic emitter resistance*, $r_e \equiv dV_{BE}/dI_E$, near room temperature is:

6.14 Dynamic emitter resistance (300K):
$$r_e = \frac{dV_{BE}}{dI_E} = \frac{k_B T}{q_e I_E} = \frac{26\,\Omega}{I_E/\text{mA}}$$

So if the emitter current is, for example, 2 mA, then $r_e = 13\,\Omega$. The dynamic emitter resistance may be thought of as a small resistor added in series with the emitter terminal just inside the transistor so that the junction V_{BE} can still be treated as a constant — actual small variations in its value connected with changes in I_E are then accounted for by a varying voltage drop across r_e. Consequently, the common-emitter amplifier gain when $R_E = 0$ is:

6.15 Common-emitter voltage gain limit (R_E = 0):
$$G \equiv dV_C/dV_B = -R_C/r_e$$

An example of a high-gain common-emitter circuit will be presented in the next section.

Simple high-gain amplifier stage

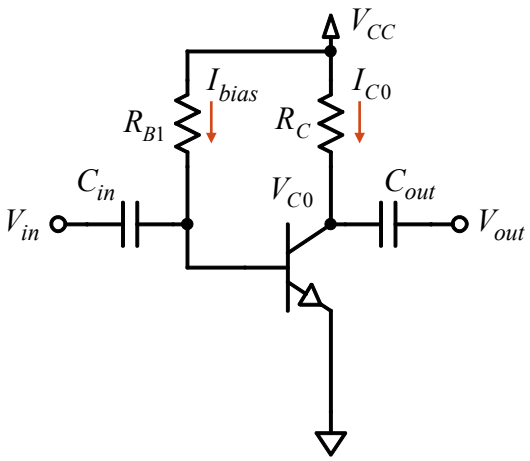


Figure 6-5: High-gain *NPN* common-emitter amplifier stage.

Although the high-gain amplifier circuit shown in Figure 6-5 is much simpler than the basic amplifier design of Figure 6-4, it will be quite dependent on the actual transistor β for its DC bias conditions and its resulting gain and output voltage range. The absence of an emitter resistor means that the transistor's dynamic emitter resistance r_e will determine the circuit gain along with the collector resistor R_C (using equations (6.14) and (6.15) on page 6-11).

The design process is similar to that used for the common-emitter amplifier of the last section, but is considerably simplified. Assuming that the transistor β is reasonably large, then we can substitute I_C for I_E in equation (6.14); substituting for r_e in equation (6.15) results in an equivalent expression for the circuit gain:

6.16
$$-G = \frac{R_C}{26\Omega} \times \frac{I_C}{\text{mA}}$$

The gain is completely determined by the voltage drop across R_C. Since $R_C I_C = V_{CC} - V_C$, we can express the gain in the equivalent form:

6.17
$$-G = \frac{V_{CC} - V_C}{0.026\text{V}} \approx \frac{V_{CC} - V_{C0}}{0.026\text{V}} \quad \text{("quiescent" voltage gain)}$$

Again, the circuit output impedance is R_C; choosing this value and the gain G determines I_{C0}. Now use the transistor β to calculate $I_{B0} = I_{C0}/\beta$. The transistor emitter is connected directly to ground, so the base bias is one diode-drop higher: $V_{B0} = 0.7\text{V}$. These two values determine the base bias resistor: $R_{B1} = (V_{CC} - V_{B0})/I_{B0}$. Substituting from the above equations,

6.18
$$\frac{R_{B1}}{R_C} = \frac{\beta}{|G|} \times \frac{V_{CC} - 0.7\text{V}}{0.026\text{V}}$$

Note that equation (6.18) also shows that once you have chosen values for R_{B1} and R_C, the amplifier's actual gain will be proportional to the transistor β. If you build a high-gain amplifier, the actual transistor β will most likely deviate from the value assumed by your design; you may have to adjust the value of either R_{B1} or R_C to trim the measured V_{C0} to achieve your design target.

Finally, the input impedance will be the parallel combination of R_{B1} and βr_e; the coupling capacitors will then determine the circuit's low-frequency performance in the same way as was the case for the previous amplifier design, as with equations (6.11) and (6.12).

The input stage of an op-amp (in its most basic form) consists of a two-transistor differential amplifier stage; it acts as a low-gain common emitter stage for a *common-mode* input ($R_C / R_E \sim 1$ if the same voltage is applied to both the + and − inputs), but acts in a high-gain amplifier configuration for a *differential* voltage input. The design of a simple differential amplifier using two *NPN* transistors is presented in the section starting on page 6-24.

TRANSISTOR SWITCH CIRCUITS

The transistor as a switch

If you apply a fairly large current to a transistor's base (a few mA, say), then $I_C = \beta I_B$ could be quite large. Consider the circuit in Figure 6-6, for example. The transistor's base-emitter junction is clearly forward-biased by the +5V V_{in} source; with $V_{BE} \approx 0.7\text{V}$, the base current would be

$$I_B = (5\text{V} - 0.7\text{V})/4.3\text{k}\Omega = 1\text{mA}$$

If the transistor $\beta \sim 150$, then we would expect a collector current of $I_C \approx 150\text{mA}$. But the collector power supply (V_{CC}) is only +5V, so with $R_C = 1\text{k}\Omega$ the most current that could possibly flow into the collector is $5\text{V}/1\text{k}\Omega = 5\text{mA}$. In this case the transistor will be driven into *saturation* by the large base current, and it will reduce its collector-emitter voltage drop (V_{CE}) to a fraction of a volt as the collector current is maximized (given the maximum current constraint V_{CC}/R_C). The transistor's operating state in this case is represented by the very left edge of the graph of the characteristic curves in Figure 6-2 on page 6-3: the region where V_{CE} is small. This region has been expanded in Figure 6-7. Note how a relatively modest base current I_B (0.2 mA) can drive this particular transistor's V_{CE} to a very small value when the maximum collector current is limited by external components to be much less than βI_B.

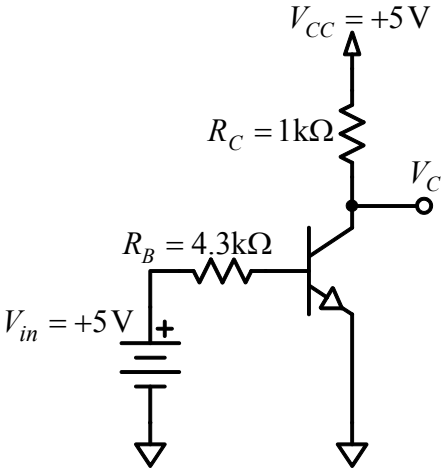


Figure 6-6: An *NPN switch* circuit.

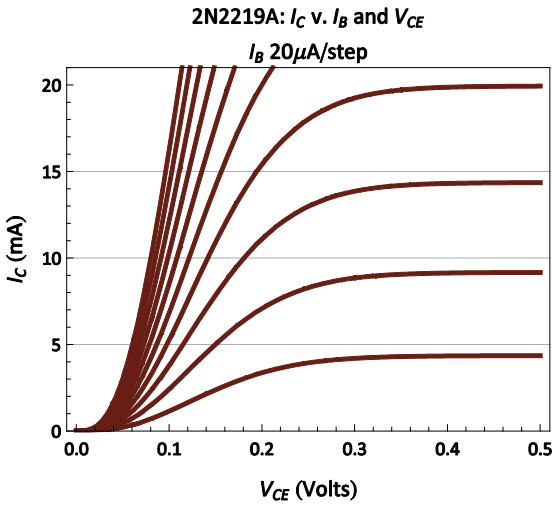


Figure 6-7: *Saturation region* of the transistor characteristic curves. The left-most curve corresponds to I_B = 0.2mA; note that even this relatively small base current will drive the collector-emitter voltage drop down to only about 0.1V even for collector currents as high as 20mA.

Ensuring transistor saturation

When using a transistor as a switch a good rule of thumb is to design the input circuit to the base so that I_B will be approximately 5% to 10% of the required I_C, ensuring that $I_C \ll \beta I_B$. This will drive the transistor well into its saturation region, minimizing V_C.

Basic switching circuits

The use of a transistor as a switch was discussed earlier; the gist of that presentation is that when acting as a switch the transistor is either: (1) *off*, because the base-emitter junction does not have a sufficient forward-bias voltage applied to it; or (2) *saturated*, because a large base-emitter forward-bias current is applied.

Consider the use of an NPN transistor switch to apply power to a load such as an LED or relay as in Figure 6-8. By driving the transistor into saturation, nearly the entire power supply voltage V_{CC} is available to supply the load connected between the collector and the power supply; relatively large currents may be passed through the transistor collector without causing overheating because $V_{CE} < 1\text{V}$ when the transistor is saturated (the PN2222A transistor, for example, can easily handle collector currents of a few hundred milliamps).

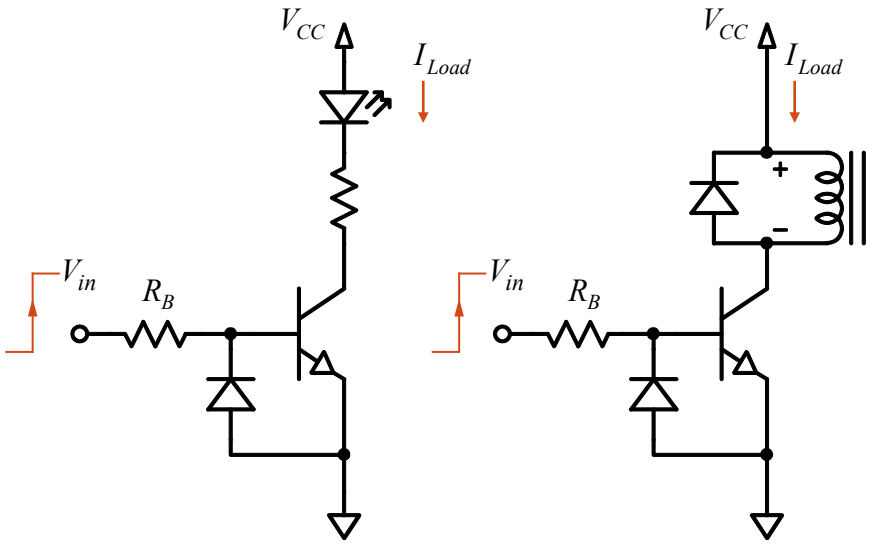


Figure 6-8: Examples of circuits using an *NPN* transistor switch: driving an *LED* or a relay coil. Bright *LED*s may require currents of several tens of mA at relatively low voltages; the same is true for some popular relays. The 10 mA output of the TL082 op-amp is not suitable for such loads, so using a transistor switch is a possible solution. The diodes across the transistors' base-emitter junctions prevent negative input voltages from causing reverse breakdown of the base-emitter *PN* junction. Note that these diodes are reverse-biased for positive input voltages, but conduct if the base voltage reaches –0.6V. The reverse-biased diode across the relay coil in the right-hand circuit prevents the large *back-EMF* from the coil's inductance from damaging the circuit when the transistor is turned off.

The base-emitter junction of the transistor has a relatively small reverse-breakdown voltage (only 6V for the PN2222A), so adding a reverse-biased diode across the transistor's base-emitter junction as shown in Figure 6-8 serves to protect the transistor from excessive negative input voltages (such as a saturated op-amp comparator output). The diode begins to conduct as the transistor base voltage reaches –0.6V, keeping the base well away from its reverse breakdown voltage limit.

Using the ***Ensuring transistor saturation*** rule of thumb makes switch circuit design straightforward, as in the following example:

EXAMPLE: SWITCHING AN *LED*

Assume that you need to switch a 30 mA green *LED* using the output of a TL082 op-amp Schmitt trigger circuit. The *LED* will have a forward voltage drop of about 2.2V when conducting 30mA, and you wish to use a 5V power supply for V_{CC}. According to the PN2222A transistor data sheet, the saturation $V_{CE} < 0.1\text{V}$ for $I_C = 30\text{mA}$ and $I_B = 3\text{mA}$ (10% of I_C as recommended by our design rule of thumb). Consider the left-hand circuit in Figure 6-8; assuming that the op-amp comparator's positive output voltage is 11V (V_{in}) when supplying a 3 mA load (the switch transistor's base circuit is the comparator's load), then the base resistor value may be calculated to set this current to the desired 3mA:

$$R_B = (11\text{V} - 0.7\text{V})/3\text{mA} = 3.43\text{k} \rightarrow 3.3\text{k}$$

The resistor R_B will dissipate less than 0.03W when conducting 3 mA, so a 1/4W resistor will work. The resistor in series with the *LED* load may also be calculated by considering the voltage drop it must have when conducting the 30 mA *LED* current:

$$R_{LED} = (5\text{V} - 2.2\text{V})/30\text{mA} = 93\Omega \rightarrow 91\Omega$$

This resistor will dissipate under 0.1W when the *LED* is illuminated, so a 1/4W resistor will work fine here also.

Generating digital logic levels from analog signals; simple logic circuits

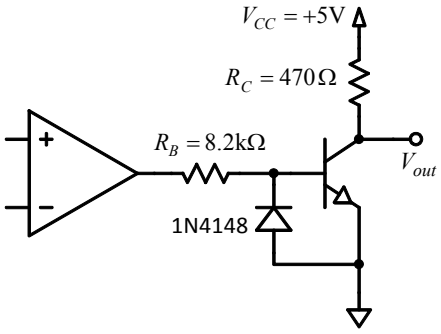


Figure 6-9: A transistor switch added to a TL082 op-amp comparator output may be used to translate the op-amp's saturated output levels of ±11V to the 0V-5V levels used by many logic circuits.

A common digital logic standard uses +5V for a logic "1" signal and 0V for a logic "0" (actually, "1" may be in the range 2.0V–5.0V and "0" is 0V–0.8V, depending on the particular *logic family* to which you are interfacing). Using a transistor switch to generate these levels is straightforward (Figure 6-9). See if you can confirm that the circuit will work properly. Note that the output of the switch is inverted: positive op-amp saturation corresponds to $V_{out} \approx 0\text{V}$, negative op-amp saturation to $V_{out} = 5\text{V}$. With the selected value $R_C = 470\,\Omega$, the current through R_C and the transistor's collector will be approximately 10mA when the transistor is saturated (on).

R_C in Figure 6-9 is called a *pull-up resistor* because it "pulls" the output voltage up to V_{CC} when the transistor turns off. Since V_{CC} is supplied to the switch's output load through this pull-up resistor, you must make sure that the current drawn by the load does not cause the output voltage to *droop* below the required logic "1" voltage level (R_C is the circuit's *output impedance* when in the logic high state); this will usually not be a problem if the load is an input to a member of the *TTL* or *CMOS* logic families. If the load does require a significant amount of current when the switch output is high (more than 1 or 2 mA), then a simple solution is to use a switch constructed from a PNP transistor.

The requirement to interface an op-amp comparator's output to the voltage levels required by digital logic circuitry is so common that entire families of special integrated circuits to perform this task have been developed by nearly all analog device manufacturers: the *comparator* ICs. One of the first truly successful comparator ICs was introduced many years ago by National Semiconductor (now a part of Texas Instruments): the LM311 (data sheet) which incorporates a flexible transistor switch into its comparator output as shown in Figure 6-10. Although venerable, the LM311 is still a useful device to include in your design "toolbox."

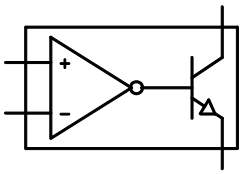


Figure 6-10: The LM311 Comparator IC (introduced in 1969) incorporates a transistor switch with an op-amp comparator. As can be seen in the simplified functional schematic, both the output transistor's collector and emitter are accessible for incorporation into a circuit design; the output transistor is turned on (transistor collector shorted to its emitter) whenever the *–Input* voltage exceeds the *+Input* voltage.

Simple logic operations using transistor switches

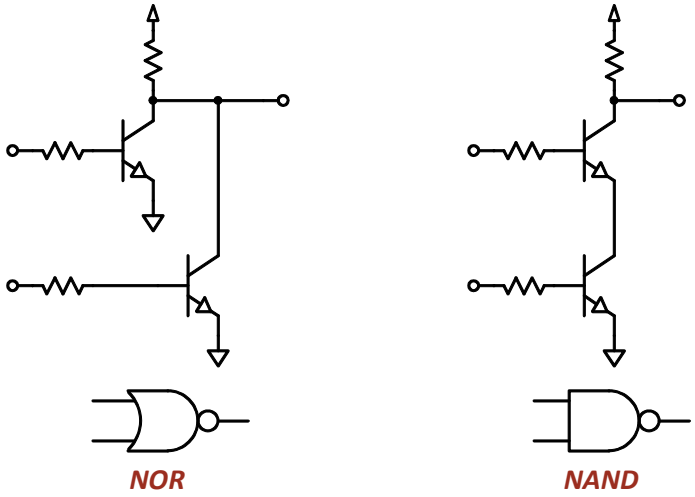


Figure 6-11: Simple logic operations implemented using basic *NPN* switch circuits.

Multiple transistor switch circuits using a common collector pull-up resistor may be used to perform simple logic operations as shown in Figure 6-11. In the case of the *NOR* configuration, if either of the transistor bases receives a *high* input, its transistor saturates and brings the output *low* (near ground potential). For the *NAND* circuit, both transistors must have their bases *high* for the output to be *low*, since the transistors are in series. More inputs could be added to either circuit. The collector resistor could be replaced by a load such as an indicator light, relay, or motor; in this case the logic operations would be *OR* and *AND*.

If more complicated logic operations are required, then the design should probably use digital logic ICs rather than logic constructed from discrete transistors and resistors. A final transistor switch could then be used if the load requires a high voltage or large current.

PRELAB EXERCISES

1. You are required to design a common-emitter amplifier (Figure 6-4 on page 6-7) with an inverting gain of 10 using a single +12V power supply ($V_{CC} = +12\text{V}$), and with an output impedance of 1kΩ.

   (1) What should be the values of R_C and R_E?

   (2) Using the design rules in the text, what is the maximum achievable output peak-to-peak voltage swing?

   (3) What should be the design quiescent collector and emitter voltages (V_{C0} and V_{E0})?

2. Continuing the above common-emitter amplifier design problem,

   (1) What will be the quiescent collector current I_{C0}? If the minimum expected transistor $\beta = 150$, then what will be I_{B0}, and what should be the minimum current through resistor R_{B2} (Figure 6-4)?

   (2) What is the target value for V_{B0}? Of the following pairs of values, which pair would make the best choice for R_{B1} and R_{B2}:

   (130 kΩ and 150 kΩ), (91 kΩ and 10 kΩ), (30 kΩ and 3.3 kΩ), (11kΩ and 1.3 kΩ)?

   (3) What will be the amplifier's input impedance?

3. Concluding the common-emitter amplifier design problem,

   (1) What will be the low-frequency −3dB corner of the amplifier's input if $C_{in} = 0.1\mu\text{F}$?

   (2) What will be the low-frequency −3dB corner of the amplifier's output if $C_{out} = 0.01\mu\text{F}$ and the load impedance $Z_{load} = 100\,\text{k}\Omega$?

4. Draw a complete schematic of the amplifier you've designed (Figure 6-4) with all component values specified. You will use a PN2222A transistor for the amplifier.

5. Consider a high-gain amplifier circuit (Figure 6-5 on page 6-12) with $R_C = 1\text{k}\Omega$ and $V_{CC} = +5\text{V}$. If the gain of the amplifier is to be $G = -100$ and the transistor $\beta = 200$, then what should be the value of R_{B1}? What will be the values of I_{C0} and V_{C0}?

LAB PROCEDURE

Common-emitter amplifier

Construct the common-emitter amplifier you've designed in Prelab exercises 1 through 4. Be sure you use the PN2222A transistor data sheet to properly identify the transistor's emitter, base, and collector leads.

This design calls for $V_{CC} = +12\text{V}$ and $V_{EE} = 0\text{V}$ (ground). With no input signal, measure the transistor's terminal bias voltages V_{C0}, V_{E0}, V_{B0}. How do they compare to your design values?

Apply an input signal and measure the amplifier's gain at 15 kHz. Increase the input amplitude until you find the amplifier's maximum output peak-to-peak voltage range. Find its low-frequency −3 dB corner.

This amplifier has a $Z_{out} = R_C = 1\text{k}\Omega$. For a high-frequency application driving a BNC cable, the cable's $\sim 100\,\text{pF/meter}$ capacitance will form a low-pass filter with the amplifier's 1 kΩ Z_{out}, limiting its high-frequency response. Check this statement by connecting the amplifier output to the DAQ using a BNC cable about 5 ft long. Use the DAQ to measure the amplifier's frequency response over the range 500 Hz – 1 MHz and determine its high-frequency −3 dB corner. What is the amplifier's gain at 1 MHz? To correct this situation the amplifier needs a lower output impedance, which we can accomplish by adding an emitter follower output stage.

Adding an emitter follower output stage

An emitter follower amplifier stage has a gain of +1 and low output impedance (equations (6.1) and (6.5)). Add an emitter follower stage to the common-emitter amplifier to lower its output impedance and thus improve its high frequency performance (the modified circuit is shown in Figure 6-12 on page 6-21).

Consider the operation and biasing of the 2-stage amplifier circuit in Figure 6-12. The biasing and operation of the common emitter amplifier (Q_1 and its biasing resistors) is just the same as for the original single-transistor amplifier. The base bias of the emitter follower transistor (Q_2) is set by Q_1's collector circuit; the base bias current Q_2 draws from that circuit should be much smaller than Q_1's collector current (5 mA), so it should have only a small effect on the high-gain stage operation. Thus the base bias voltage of Q_2 is set to equal the collector bias voltage of Q_1, which should be about 6.75V according to the solution to prelab exercise 1(3).

The emitter voltage of Q_2 should be approximately 0.7V less than this, or about 6V. The Q_2 emitter bias current is then set by the value of R_E; choosing $R_E = 3.0\text{k}$ will establish a reasonable bias current of around 2 mA. Assuming the transistor $\beta \sim 150$, what is the base current Q_2 would then draw from Q_1's collector circuit? Should this current indeed have

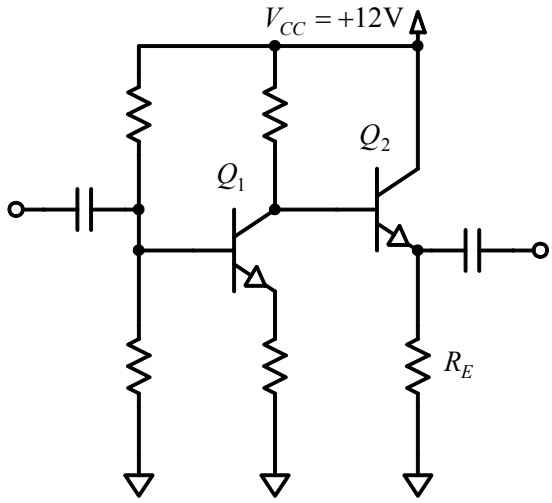


Figure 6-12: Adding an emitter follower output stage to the common emitter transistor amplifier circuit. The added components are transistor Q_2 and its emitter resistor R_E. The output coupling capacitor is moved from the collector of Q_1 to Q_2's emitter.

only a small effect on Q_1's biasing as we assumed? What should be the output impedance of this emitter follower stage? By about what factor should this raise the high-frequency cutoff of the (amplifier + BNC + DAQ) combination (actually, another factor also limits the high-frequency performance of the amplifier: the capacitance of the transistor's base-collector *PN* junction.

Build and test the operation of this 2-stage amplifier. Use the DAQ to measure the modified amplifier's frequency response over the range 500 Hz – 1 MHz. What is the amplifier's gain at 1 MHz? How does this compare to the original, single-stage amplifier's performance?

High-gain amplifier

Construct the high-gain, NPN transistor amplifier (Figure 6-5 on page 6-12) with the specifications provided by Prelab exercise 5. Remember, this new circuit calls for $V_{CC} = +5\text{V}$. Measure V_{C0} and adjust the value of R_C to better achieve your design value. Calculate a new gain estimate from your final V_{C0} value (see equation (6.17)).

The gain of this amplifier is large (~ 100), but its maximum output voltage range is only $\sim 4\,\text{V}$ pk-pk ; make sure that you use an input signal which is small enough that the amplifier output is not saturated. Measure the amplifier's gain at 10 kHz and determine its low-frequency −3 dB corner.

Increase the input amplitude until you find the amplifier's maximum output peak-to-peak voltage. Does the output waveform appear distorted even when you are below this maximum? What could be causing this behavior?

Transistor switch

Construct a transistor switch to illuminate an LED with a 30 mA current from the +5V power supply (see Figure 6-8 on page 6-15 and the Example: Switching an *LED* on page 6-16) when driven by a saturated op-amp output such as from the Schmitt trigger circuit of Experiment 4, Figure 4-3 on page 4-3. Don't forget to include the base-emitter protection diode shown in Figure 6-8 – use a 1N4148 or 1N914 for this diode.

Additional circuits

If you have time, attempt to build one or more additional circuits and test their operation. Use examples from the ***More circuit ideas*** section, from previous experiments, or try one of your own design.

Lab results write-up

As always, include a sketch of the schematic with component values for each circuit you investigate, along with appropriate oscilloscope screen shots. Make sure you've answered each of the questions posed in the previous sections.

MORE CIRCUIT IDEAS

Phase Splitter

Figure 6-13 shows a simple circuit from *Horowitz and Hill* which combines common-emitter and emitter follower ideas to provide two equal-amplitude, opposite-phase outputs. By choosing $R_C = R_E$ (and both $\gg r_E$), the gain to each output is 1, but the collector and emitter voltages will vary out of phase with each other. Shown here using bipolar (±12V) power supplies, the voltage swing from either output can nearly reach ±6V as the transistor operating state varies from cutoff to saturation. Of course, the base bias resistors R_{B1} and R_{B2} must be chosen to set the base voltage to $V_{E0} + 0.7\text{V} = -5.3\text{V}$, and the coupling capacitors' values set the circuit's low-frequency cutoff.

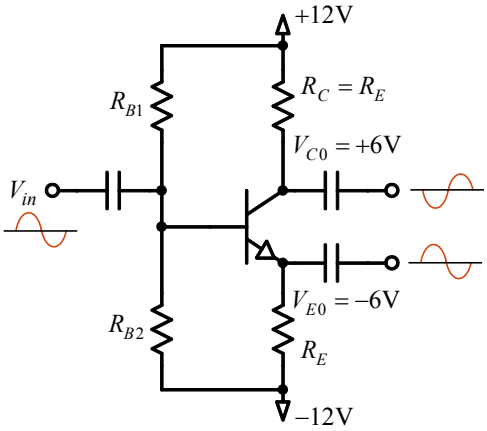


Figure 6-13: Phase splitter. Outputs are 180° out of phase.

Using PNP transistors

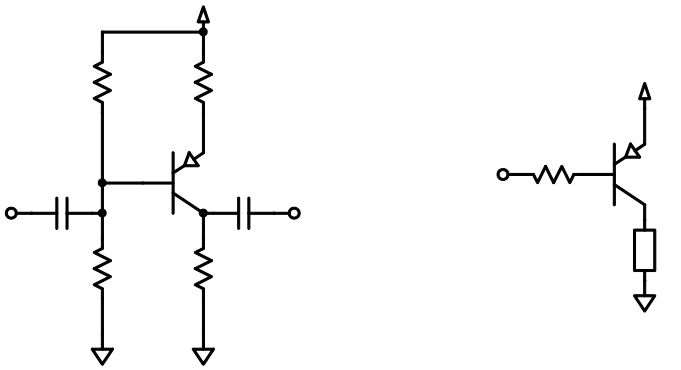


Figure 6-14: *PNP* versions of a common-emitter amplifier (left) and a transistor switch (right). The power supply voltage is >0 and is indicated by the upward-pointing arrows in the circuits. In the case of the switch, pulling the input *low* (to ground) will turn the transistor on and connect its load to the power supply. Note that unlike the *NPN* switches shown in Figure 6-8, the load of a *PNP* switch may have one terminal connected to ground, and a large current may then be supplied when the output is *high*.

In a *PNP* transistor the roles of conduction electrons and holes in the various regions of the transistor's semiconductor material are reversed; consequently the externally-applied bias voltages and resulting currents change sign from those for the *NPN* transistor. Figure 6-14 shows *PNP* versions of amplifier and switch circuits; note that they are derived from the corresponding *NPN* circuits by reflecting those circuits vertically (top for bottom) and changing the transistor type. The type 2907 transistor may be used as a *PNP* counterpart of the type 2222 *NPN* transistor.

A differential amplifier stage

A differential amplifier suitable for use as the input stage of a simple op-amp is shown in Figure 6-15. Two matched transistors are arranged in identical common-emitter configurations which share the emitter resistor R_E. The output is taken from one of the two amplifiers, whose input then becomes the *–Input* of the differential stage. The object of the amplifier circuit is to have a high gain for a differential input signal, $V_{in+} - V_{in-}$, but have a much smaller output in response to a common-mode signal, $V_{in+} = V_{in-}$. In addition, the amplifier should be able to respond to DC (or very slowly changing) inputs, so it must be *directly coupled* — no capacitors may be used to isolate the amplifier stage's inputs from its required DC bias voltages.

Consider the design shown in Figure 6-15. Note that bipolar (both + and −) power supplies are used so that the transistor bases can still be biased properly when they are directly connected to 0V low-impedance inputs (grounds). This characteristic will satisfy the last criterion listed above: direct coupling of the input stage to the signal inputs. When both inputs are connected to ground, the resultant quiescent operating state currents and voltages are indicated in the right-hand diagram in Figure 6-15. Since both halves of the circuit are identical, so will be the corresponding currents and voltages on the two sides.

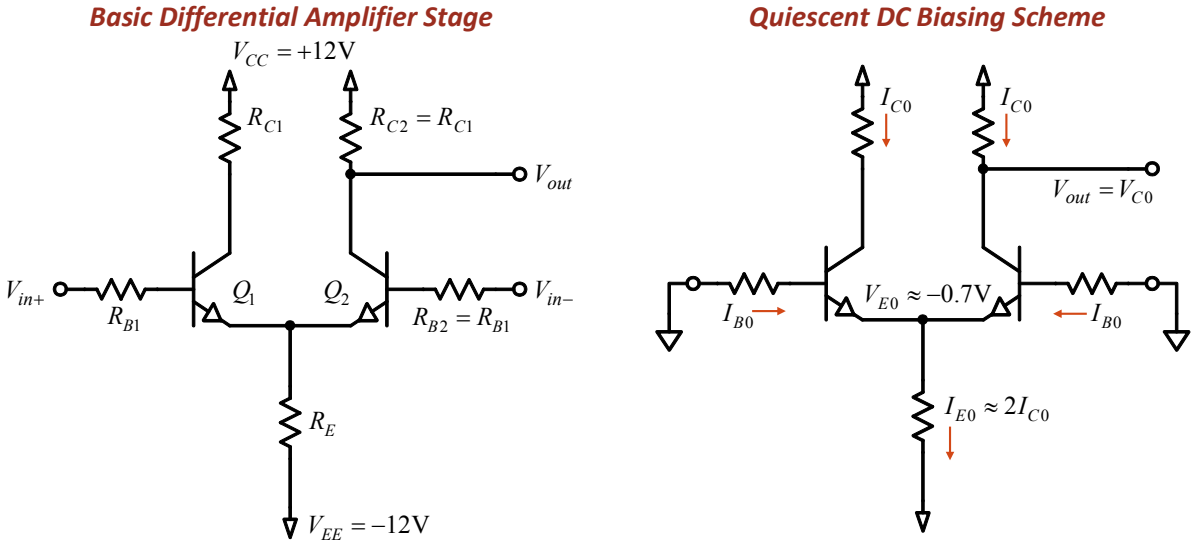


Figure 6-15: A basic *NPN* transistor differential amplifier stage, suitable for use in a simple operational amplifier design. Component and terminal identifications are shown on the left, quiescent bias currents and voltages on the right (for 0V DC inputs).

A good operational amplifier should have a high input impedance and small input bias currents; this may be accomplished by choosing a large value for R_E: a few MΩ will suffice for this simple circuit. Because the voltage drop across R_E is approximately equal to V_{EE}, the bias current through I_{E0} will then be a few microamps; the currents into the two transistor bases will be $\sim\beta$ times smaller, so the input bias currents should be less than 10^{-7} amps. The

base resistors R_{B1} and R_{B2} are required to provide some protection to the transistors in the event that the differential input voltage is large; they should have values of ~10k, so the voltage drops across them due to the input bias currents will be on the order of a millivolt or less. Thus we can ignore them for now. The collector resistors, R_{C1} and R_{C2}, set the collector bias voltages and will determine the circuit's differential and common-mode gains. Since the combined emitter bias current I_{E0} will be divided equally by the two identical halves of the circuit, we get $V_{C0} = V_{CC} - (I_{E0}/2)R_{C2}$: this will also be the quiescent output voltage with both inputs grounded.

To determine the behavior of the differential amplifier when nonzero input signals are present, we analyze its response to two different input conditions: $V_{in+} = V_{in-}$ (a common-mode input signal) and $-V_{in+} = V_{in-}$ (a differential input signal). By linear superposition of these two results we can predict the circuit's response to any arbitrary combination of V_{in+} and V_{in-} signals.

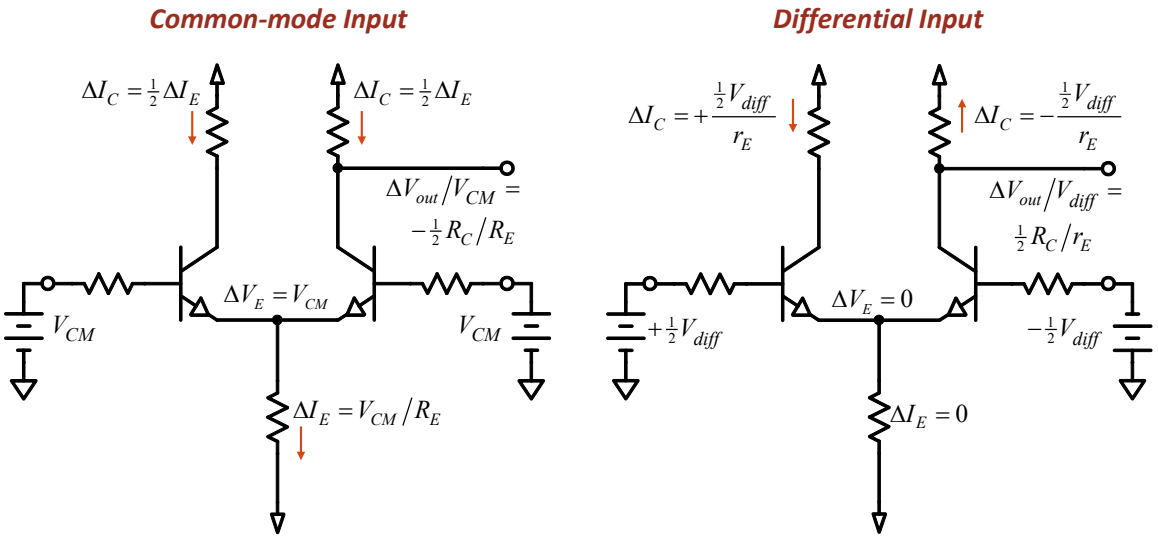


Figure 6-16: Responses of the differential amplifier stage to common-mode (left) and differential (right) inputs. The currents and voltages shown are the changes to the quiescent operating state values shown in Figure 6-15.

Consider the common-mode input first, shown in the left-hand diagram of Figure 6-16. In this case the same voltage is added to both transistor bases, and, since the base-emitter voltage drop of 0.7V is maintained, the voltage across the emitter resistor must change by the same amount. The resulting increase in the emitter resistor current, ΔI_E, is divided equally between the two transistors because of the symmetry in the circuit. Ignoring the small base currents, half of ΔI_E then appears across each of the collector resistors, and the resultant change in the voltage drop across R_{C2} appears at the circuit's output. Thus the common-mode voltage gain $g_{CM} = -\frac{1}{2}R_C/R_E$, as shown in Figure 6-16.

The gain of the circuit to a differential input may be similarly analyzed using the right-hand diagram in Figure 6-16. In this case equal and opposite voltages are applied to the inputs, resulting in equal and opposite changes in the transistors' base biases. Thus the emitter currents will also change in opposite directions, and the total current through R_E remains constant (to first order in the assumed small differential input voltage). This implies that the emitter voltage of each transistor doesn't change, so we have a situation identical to that of the high-gain common-emitter amplifier in Figure 6-5. Each transistor input sees one half of the total differential input voltage, and the gain of each is determined by the ratio of its collector resistor to its dynamic emitter resistance: $r_E = (26\,\Omega\,\text{mA})/I_{C0}$. Consequently, the differential voltage gain $g_{diff} = \frac{1}{2} R_C / r_E = \frac{1}{2} I_{C0} R_C / 26\text{mV} \approx 20 \times (V_{CC} - V_{C0})$ (voltages in volts). Typically, with $V_{CC} \sim 10\text{V}$, we would get $g_{diff} \sim 100$.

The *common-mode rejection ratio* (*CMRR*) of a differential amplifier stage is defined to be the ratio of these two gains: $CMRR \equiv \left| g_{diff} / g_{CM} \right|$. For the case of our simple differential amplifier stage, Figure 6-15 and Figure 6-16,

$$CMRR = \frac{R_E}{r_E} = \frac{I_{C0} R_E}{26\,\text{mV}} = \frac{\frac{1}{2} I_{E0} R_E}{26\,\text{mV}} \approx 20 \times (|V_{EE}| - 0.7)$$

where V_{EE} is measured in volts. For our example, $CMRR \approx 20 \times 11.3 \approx 226 = 47\,\text{dB}$, not bad for two transistors and a few resistors. This ratio can only be achieved in practice, however, if the two halves of the circuit are very well matched; if not, then the two collector currents will differ somewhat, and our assumption of perfect symmetry between the two halves of the circuit will be invalid: because of the mismatch, a common-mode input will generate a small differential signal in the two transistors' emitter circuits as well, and this error will reduce the *CMRR*.

Boosting op-amp output power

If you need your circuit output to supply more than about 10mA, the standard TL082 op-amp's output is insufficient. To quickly fashion together a "power op-amp" which can supply higher currents (100mA or so), you can add an emitter follower transistor amplifier to the op-amp's output. To enable this added amplifier to supply both positive and negative output voltages into a load, we can use both *PNP* and *NPN* transistors in a so-called *push-pull* emitter follower circuit as shown in Figure 6-17.

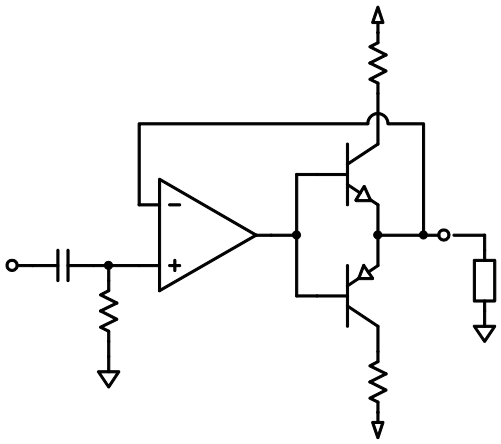


Figure 6-17: A simple *push-pull* emitter follower circuit uses a *complementary pair* (*NPN* and *PNP*) of transistors to boost the output current of an op-amp. Note that the negative feedback is from the transistors' output (the little hump in the feedback wire as it crosses below the resistor means that there is no connection between the crossing wires). The collector resistors reduce the transistors' power dissipation when driving a low-resistance load.

Because (1) the feedback loop includes the transistors and (2) the op-amp adjusts its output voltage to keep its two inputs equal, the output voltage applied to the load should follow the input voltage to the op-amp +*Input*. When the input is positive, then the op-amp raises its output voltage until the upper, *NPN* transistor turns on, supplying current to the load from the positive power supply. Since this requires that the base-emitter junction is forward-biased at about 0.7V, the op-amp output voltage must be maintained 0.7V higher than the voltage applied to the load. This reverse-biases the lower, *PNP* transistor base-emitter junction, so that transistor is turned off. Conversely, when the input voltage goes negative, the op-amp slews its output to 0.7V below the desired load voltage, activating the lower, *PNP* transistor and turning off the *NPN* transistor. Thus the two transistors alternate between inactive and conducting on alternate half-cycles of the input waveform, a mode of operation commonly referred to as *Class B* (the amplifiers presented earlier are all *Class A*: the transistors are biased on during all normal input and output conditions).

One significant drawback of this simple, Class B power amplifier is that it introduces *crossover distortion*: glitches in the output waveform as it passes through 0. Because each transistor requires that its base-emitter junction is forward-biased by approximately 0.7V for

it to operate, there is a "dead zone" in the circuit's output whenever the op-amp is within about ±0.7V of 0. The op-amp's output must pass through this zone as rapidly as possible whenever the input passes through 0, but it is limited by its slew rate (about 13 V/µs for the TL082). Consequently, the output waveform has little "flat spots" at 0V as the op-amp slews through the required 1.4V to activate the other output transistor (Figure 6-18). A more complicated design (as used in an actual op-amp's output stage) includes some base biasing so that both transistors are properly biased when the output is near zero, eliminating crossover distortion. This modified type of amplifier designated *Class AB*, because it is a hybrid combination of classes A and B.

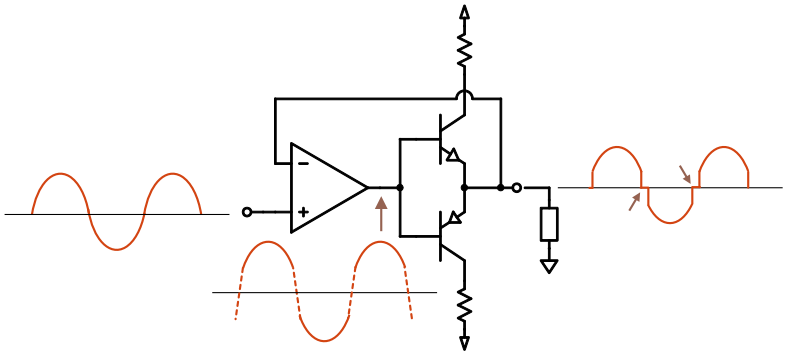


Figure 6-18: Generation of *crossover distortion* in the simple, *Class B* power-booster's output caused by the transistors' 0.7V base-emitter turn-on voltage coupled with the op-amp's finite slew rate.

If the load resistance is fairly high, so that high output currents will require that most of the transistors' power supply voltages be applied to the load, then the average power dissipated in the amplifier's transistors may be small, and the collector resistors may be omitted. If the load resistance is small, on the other hand (for example, an 8Ω speaker), and the power supply voltages are relatively high (such as the ±12V supplies on the breadboard), then the power dissipated by the transistors may be excessive.

The 250mA maximum available current from the ±12V supplies requires only 2V across an 8Ω speaker load, so the other 10V has to be dropped through the transistors and their associated collector resistors. The RMS power into the load in this case is only 0.25W, but *the average power drawn from each power supply line* is nearly 1W (for a sinusoid input only; a square wave input would draw 1.5W average). Where does all this extra power go? into heating of the transistors and their collector resistors, of course! On average each resistor-transistor combination will drop about 11V while the load draws about 100 mA; to divide this equally between the two, each collector resistor should be about 60 Ω: two 120 Ω resistors in parallel will do the trick, and they together can handle 1/2W, leaving 1/2W for each transistor.

Note that the circuit has its input AC coupled (the high-pass *RC* filter). This is so that a steady, DC input will not cause the op-amp output to saturate, turning one transistor on and causing a steady, large current flow through one half of the circuit with its consequent large power dissipation.

If a truly versatile, low distortion, high frequency, large current output is needed for your design, then the simple transistor power booster will be inadequate, and a more complicated solution is called for. An interesting design choice is to use a special purpose buffer amplifier IC such as the Linear Technologies LT1010 which can be used with an op-amp to boost its current output to 150mA. Otherwise, you may choose a high-power op-amp — the Texas Instruments OPA541, for example, can output 10A peak using ±40V power supplies! A less dramatic example is the Analog Devices AD817: a 50MHz, 350 V/μs, 50mA op-amp.